25-56 Gbps Silicon Photonics on 28nm CMOS

Sofics

ABSTRACT

In the past, Fiber-optic communication was used only for long distance communication (50 km and beyond). Only a small number of these high-end interface products were required worldwide. The suppliers could not distribute the development cost across a large volume of products. The circuits were manufactured with niche, expensive process technologies (III/V).

More recently, companies running large data centers (Facebook, Google, Amazon,...) like to replace the traditional cabling between server racks. The copper-based approach is considered a bottleneck for further improvements in data transfer capacity. Optical fiber can dramatically increase the bandwidth between servers and reduce complexity.

Thus, the optical interconnect suppliers now need to produce a large number of their products. To reduce the cost, they separate the optical parts (laser diodes, photo detectors) from the digital controller circuits. That allows to rely on advanced, standard CMOS technology for those controller circuits, enabling a cost-effective high volume production. Both elements are combined within a single IC package using advanced packing techniques. To enable the high bandwidth communication several 'lanes' of >25Gbps or 56Gbps are combined to build 100G or 200G communication lines.

The 25-56Gbps interfaces consist of SerDes-type circuits and are integrated into advanced CMOS technology like 28nm CMOS. To create such high-speed differential circuits, designers utilize the thin oxide transistors. However, those transistors are very sensitive and can be easily damaged during transient events like electrostatic discharge (ESD).

Despite the fact that the sensitive pads are not connected outside of the package, they could still receive ESD stress during assembly. Therefore, adequate protection clamps need to be inserted at the bond pads. On the other hand, for signal integrity, it is important to limit the capacitance between the interface pads and the supply lines.

Sofics has worked with several companies developing these optical interconnect interfaces. We have developed ESD protection with parasitic capacitance below 15fF, ten times lower than the typical low-cap ESD protection devices in TSMC 28nm CMOS. During the presentation Sofics will provide details about the different projects and the protection concepts used.

25-56 GBPS SILICON PHOTONICS ON 28NM CMOS

TSMC – OIP 2017

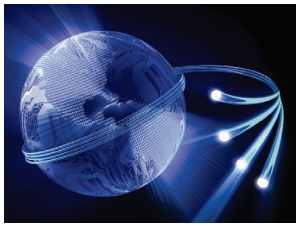
BENJAMIN VAN CAMP – CTO, SOFICS

OUTLINE: Silicon photonics

- **Introduction**
- Integrated Silicon Photonics
  - Concept
  - Requirements for the CMOS chip
  - Case studies
- Conclusions

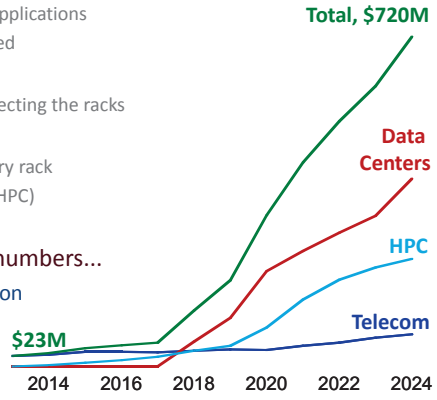
Fibre optic communication

- History
  - 1880: Photophone: transmission of sound on a beam of light
  - Developed in 1970s for telecommunications industry
  - Mostly used for long distance, high bandwidth connections
  - Major role in information age with explosive growth of data needs
- Benefits of optical communication
  - Low loss
  - Long distance between amplifiers/repeaters
  - High bandwidth
  - No cross talk
  - Immunity to electromagnetic interference
  - Light weight
  - Secure: Difficult to tap without disrupting the signal



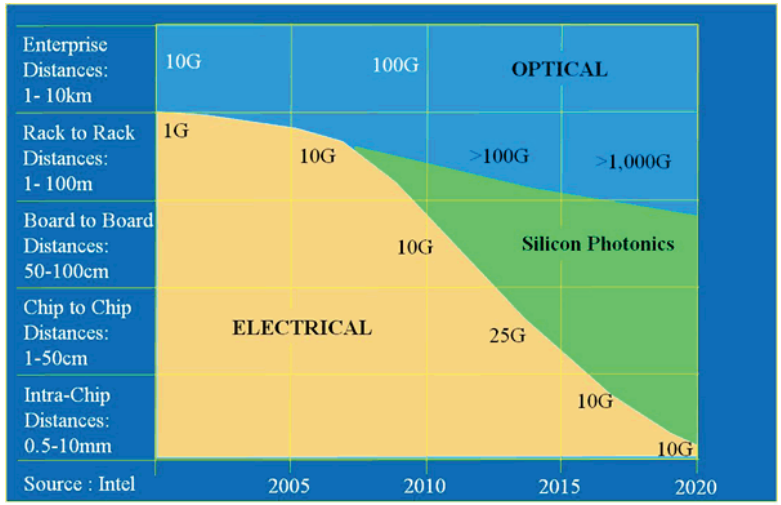
Bright future for optical communication

- Optical communication market is expected to grow strongly
  - Past:
    - Long distance, telecom, niche applications
    - Limited number of parts required
  - Today
    - Within Data Centers (DC), connecting the racks
  - Coming up
    - Between servers, boards in every rack
    - High Performance Computing (HPC)
- What is required to reach these numbers...
  - Low cost, reliable mass-production



Silicon Photonics Report—Yole Développement; Yole

Silicon Photonics to the rescue



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  - **Concept**
  - **Requirements for the CMOS chip**
  - **Case study on 28nm CMOS**
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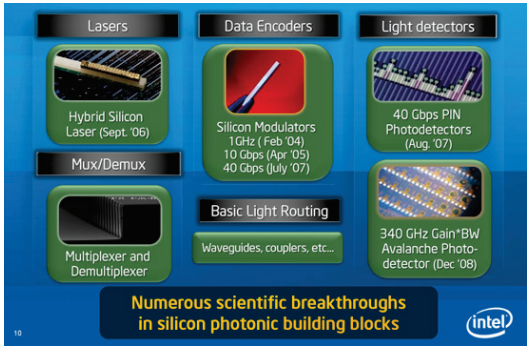
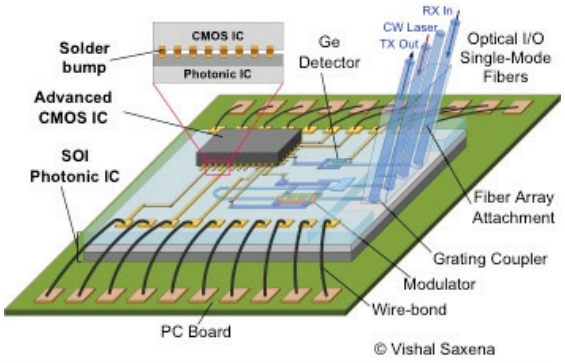
Silicon photonics substrates

- Integration of optical components on SOI substrate
  - Conventional processing steps
  - Optical components
    - WDM – Wavelength Division Multiplexing
    - Lasers, Modulators, Detectors, Waveguides ...

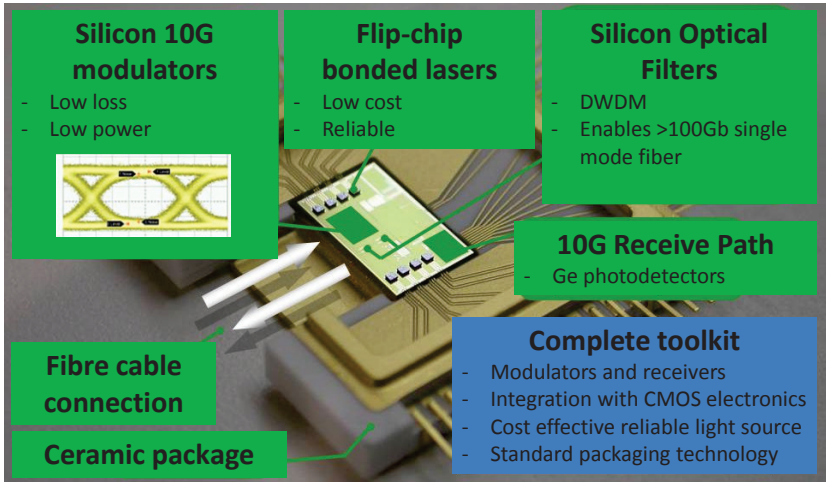


Hybrid 2.5D and 3D integration

- Enabling new markets: high bandwidth, low cost, low power
  - Functionality of conventional CMOS circuits
  - Enhanced system performance of photonic solutions.
  - Integration of optical, electronic components on silicon-based substrates

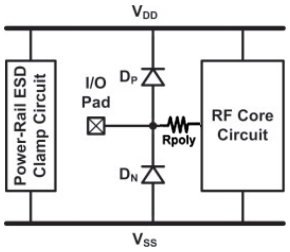


Luxtera CMOS Photonics - example



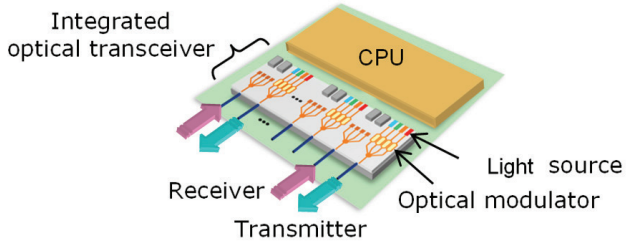
Why optical links need custom ESD clamps?

- Controlling ASIC is still an **electrical IC**
  - Based on **advanced CMOS technology**
  - ESD **sensitive transistors** need adequate protection
- Custom differential interfaces need analog IOs
  - Operated at **low voltage, below standard IO-levels**
  - Low leakage ESD clamps required
- High speed interface cannot tolerate parasitics
  - **No ESD-resistance** allowed in the pad
  - **Ultra-low parasitic capacitance** required



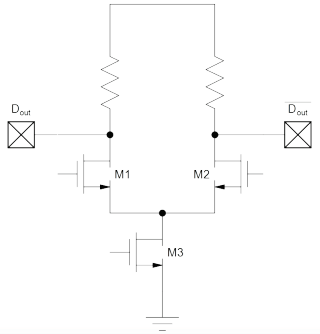
Sofics supported 7 Silicon Photonics projects

- Sofics supported projects on various CMOS nodes
  - TSMC 180nm, 130nm, 40nm
  - 3 projects on TSMC 28nm
  - SiGe BiCMOS process
- Focus on CMOS ASIC ('CPU')
  - Protect high speed interconnects (Tx, Rx)
  - Protect low voltage, thin oxide domains



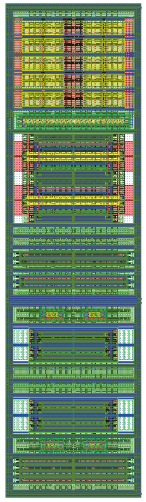
Case 1: TSMC 28nm – Requirements

- ESD requirements
  - Regular 3.3V IO circuits
    - Standard requirements: 2kV HBM
  - High speed differential circuits connect to the Photonics die
    - Ultra-low parasitic capacitance for ESD protection: maximum 20fF
    - ESD-safe assembly: Level reduced to 200V HBM

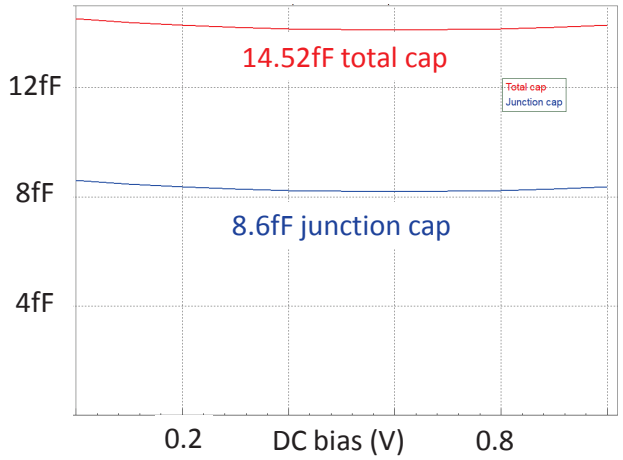


Case 1: Sofics' clamp – 28nm

- Protection of high speed pins
  - 1V input/output using 0.9V thin oxide transistors
  - Protection level
    - 200V HBM
  - Area
    - 13.66um x 50.055um = 683.75 um²
    - Full local protection and integrated power clamp
  - Leakage current
    - 10 pA at 25°C
    - 10 nA at 125°C

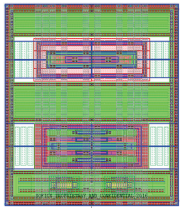


Case 1: Sofics' clamp – 28nm – Parasitic capacitance

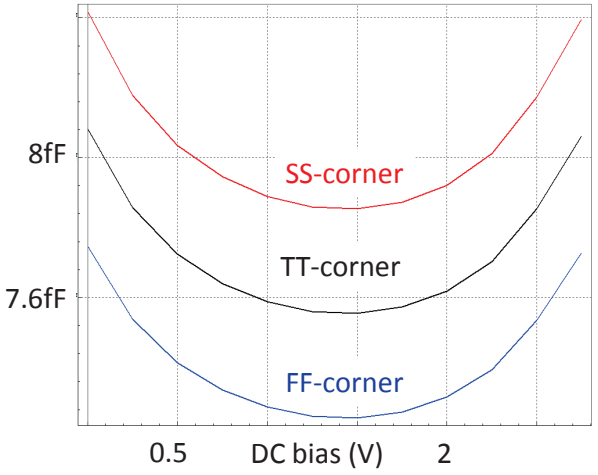


Case 2: Sofics' clamp – 28nm – Protection solution

- Protection of high speed pins
  - 1V input/output using 0.9V thin oxide transistors
  - Protection level
    - 100V HBM
  - Area
    - 13.66um x 15.875um = 216.9 um²
    - Full local protection
  - Leakage current
    - 10 pA at 25°C
    - 10 nA at 125°C

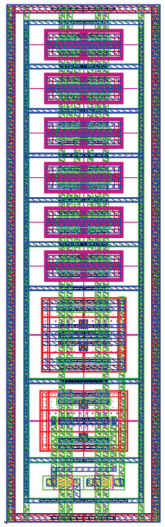


Case 2: Sofics' clamp – 28nm – Parasitic capacitance

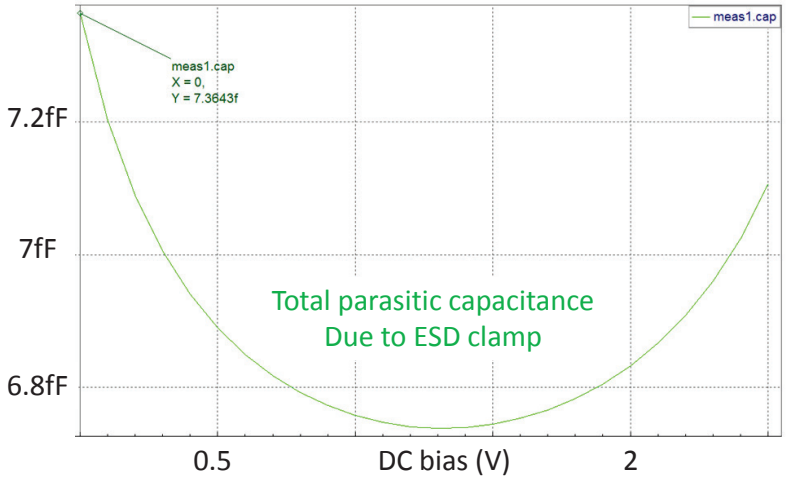


Case 3: Sofics' clamp – SiGe BiCMOS

- Protection of high speed pins
  - 2.5V inputs/outputs
  - Protection level
    - 200V HBM
  - Area
    - 11.02um x 37.3um = 412 um²
    - Full local protection and integrated power clamp
  - Leakage current
    - 10 pA at 25°C
    - 10 nA at 125°C



Case 3: Sofics' clamp – BiCMOS – Parasitic capacitance



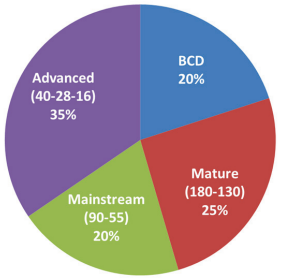
Specialty ESD clamps available on TSMC technology

- Broad solution coverage on TSMC technology
  - Silicon proven solutions, Including different flavours
  - > 250 silicon proven cells – datasheets available online
  - **Portable to other nodes/domains**

Node	Voltage domains
350nm HV	3.3V 15V
250nm BCD, gen. I and II	12V 24V 40V 60V
180nm BCD, gen. I and II	18V 24V 32V 40V 60V
180nm CMOS	1.8V 3.3V 5V
130nm CMOS	1.0V 1.2V 3.3V 5V 7V
90nm CMOS	1.2V 1.8V 3.3V
65nm CMOS	1.0V 1.2V 1.8V 2.5V 3.3V 5V
40nm CMOS	0.9V 1.2V 1.8V 3.3V 5V
28nm CMOS	0.85V 0.9V 1.8V 3.3V 5V 5.5V 12V
16nm FF+	0.8V 1.2V 1.5V 1.8V 2.5V 3.3V 5V

Open Innovation Platform®

Percentage of projects on TSMC technology nodes



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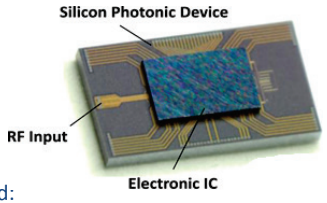
Conclusions

- Silicon Photonics enables strong growth of communications market
  - Mass production opportunity through CMOS processing
  - Hybrid 2.5D and 3D integration with CMOS ASIC

- Sofics supported 7 projects for several companies
  - 180nm through 28nm CMOS and SiGe BiCMOS
  - Ultra low parasitic capacitance of about 10fF
  - Interface speeds from 10Gbps to 56Gbps



- Future?

  In 2006 Former Intel senior VP Pat Gelsinger stated:

  "Today, optics is a niche technology. Tomorrow, it's the mainstream of every chip that we build."